

Technical Note

Calculating Memory System Power for DDR

Introduction

Today's system designer is concerned about the power used by the main memory in the system. Whether it is calculating battery life for a portable application, planning cooling for a "pizza box" desktop, or determining the power supply for a server, an accurate power budget for the memory is essential. Unfortunately, data sheets do not always make it easy to determine how much power is used by each device in a specific application.

This technical note explains how power is consumed by DDR SDRAM and provides some basic tools to help calculate the system power that is consumed by the DRAM. These tools can be adapted to fit a wide range of applications and even help identify simple methods for modifying a system to use less power without significantly affecting the system's performance. After all, a high-performance system will disappoint if it overheats or the battery life fails to meet end users' expectations.

While this technical note is targeted at tools and techniques to calculate system power, actual examples are also provided. An example of a DDR400 data sheet is provided in Appendix A, and working examples are provided in Appendix B. Values provided in data sheets may differ from vendor to vendor and over time, but the concepts behind calculating power are the same.

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DRAM Operation

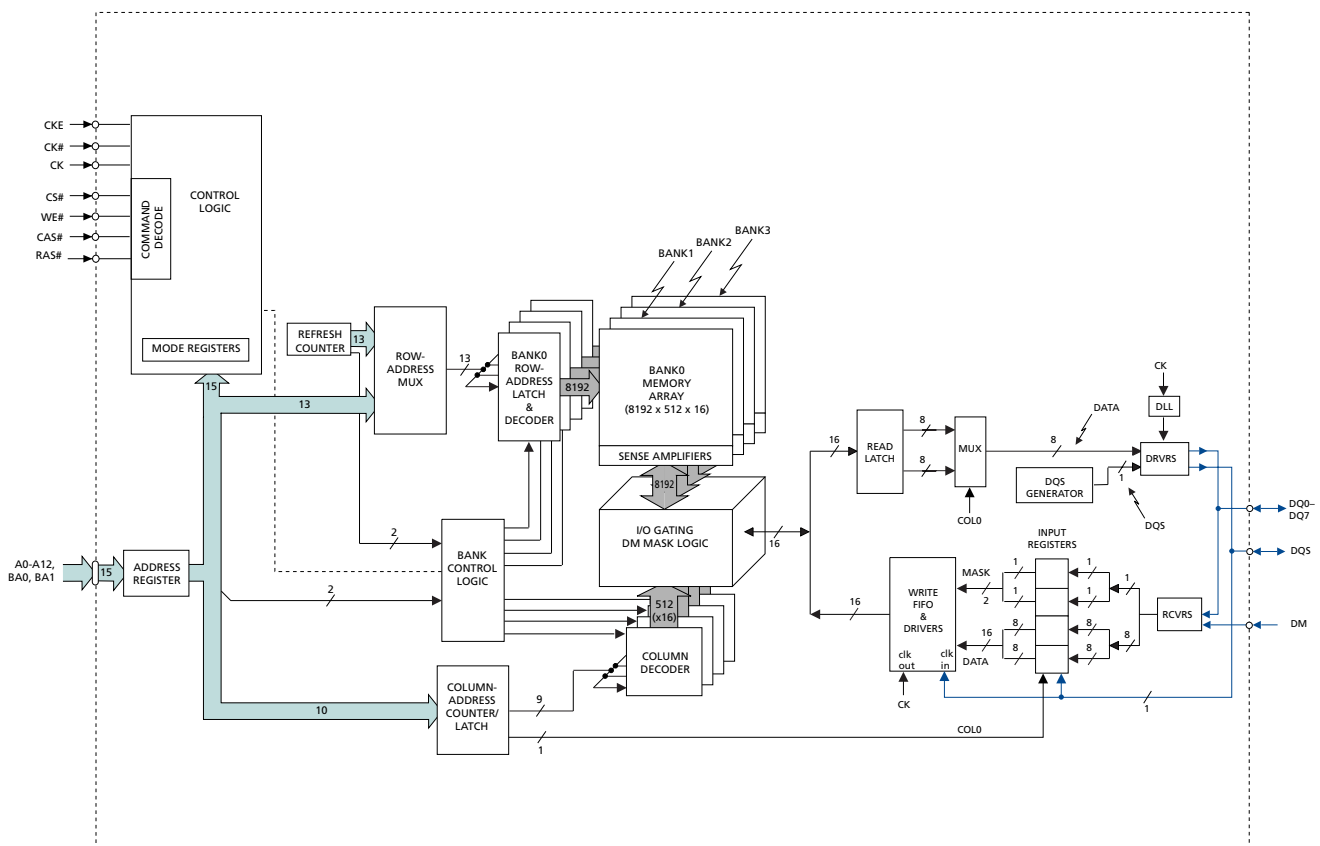
To estimate the power consumption of a DDR SDRAM, it is necessary to understand the basic functionality of the device (See Figure 1). The master operation of the DRAM is controlled by CKE (clock enable). If CKE is LOW, the DDR SDRAM clock and input buffers are turned off. To communicate with the device, CKE must be HIGH. This enables the inputs and propagates the clock through the DRAM.

Once CKE is HIGH, commands can be sent to the DDR SDRAM. Typically, the first command is ACTIVATE (ACT). The ACT command selects a bank and row address and transfers that row's cell data, which is stored in the array, to the sense amplifiers. The data stays in the sense amplifiers until a PRECHARGE command to the same bank restores the data to the cells in the array. When data is stored in the sense amplifier, the DRAM is said to be in the active state. After the data in the sense amplifiers has been restored to the memory array, it is said to be in the precharge state.

When the DDR SDRAM is in the active state, READs and WRITEs may take place. A READ command decodes a specific column along the row that is stored in the sense amplifiers. The data from this column is driven through the I/O gating to the internal read latch. Once in the latch, it is multiplexed onto the output drivers.

It is also possible to write data to the sense amplifiers while the bank is active. The process is the opposite of the read process. Data from the DQ pins is latched into the data receivers/registers and transferred to the internal data drivers. The drivers then transfer the data to the sense amplifiers through the I/O gating to the decoded column address.

Figure 1: 256Mb DDR SDRAM Functional Block Diagram



DRAM Power Calculations

For this technical note, the IDD values are shown in “Appendix A: Assumptions” on page 18. This is an extraction from a 256Mb DDR400 SDRAM data sheet. Other values may be substituted if the device data sheet is different. It is the engineer’s responsibility to verify all data sheet parameters before using this information.

CKE Operation

As stated previously, CKE is the master on-off switch for the DRAM. When CKE is LOW, all inputs, including clocks, are disabled. This is the lowest power state in which the device may operate. This power is specified in the data sheet at IDD2P if all the banks are precharged and IDD3P if any bank is active.

CKE must be taken HIGH to read or write data to the DDR SDRAM. Upon CKE going HIGH, the clock signals start propagating through the DDR SDRAM and the device is prepared to start receiving commands. This activity within the DRAM increases the power consumption and is specified in the data sheet at IDD2F if all the banks are precharged and IDD3N if any bank is active.

Figure 2 shows the typical current usage on a DDR SDRAM device when CKE is transitioned. When CKE is HIGH, the device draws approximately 40mA of current; when CKE goes LOW, it drops to 5mA.

Figure 2: Effects of CKE

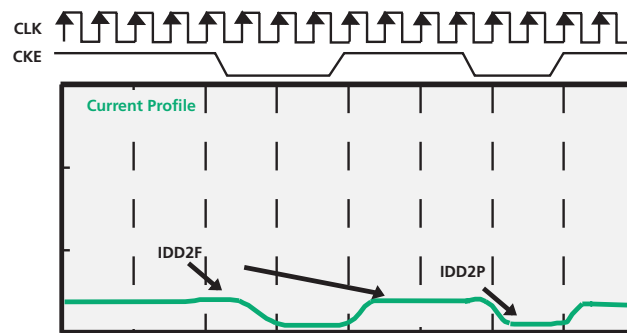


Figure 2 assumes the device is in the precharge state. Thus, when CKE is HIGH, the DDR SDRAM uses IDD2F current; when CKE is LOW, it uses IDD2P current. Similarly, if the device is in the active state, it consumes IDD3P current in power-down state (CKE = LOW) and IDD3N current in standby (CKE = HIGH).

The power consumed by the DDR SDRAM is easily calculated by multiplying the IDD values by the voltage applied to the device VDD.

$$p(\text{PRE_PDN}) = I_{DD2P} \times V_{DD} \quad (\text{EQ 1})$$

$$p(\text{PRE_STBY}) = I_{DD2F} \times V_{DD} \quad (\text{EQ 2})$$

$$p(\text{ACT_PDN}) = I_{DD3P} \times V_{DD} \quad (\text{EQ 3})$$

$$p(\text{ACT_STBY}) = I_{DD3N} \times V_{DD} \quad (\text{EQ 4})$$

Note that the data sheet values for all I_{DD} values are taken at worst-case V_{DD} , which is 2.7V for the DDR SDRAM. The equations are solved as follows:

$$\begin{aligned} p(\text{PRE_PDN}) &= 4\text{mA} \times 2.7\text{V} \\ p(\text{PRE_PDN}) &= 11\text{mW} \end{aligned} \tag{EQ 5}$$

$$\begin{aligned} p(\text{PRE_STBY}) &= 60\text{mA} \times 2.7\text{V} \\ p(\text{PRE_STBY}) &= 162\text{mW} \end{aligned} \tag{EQ 6}$$

$$\begin{aligned} p(\text{ACT_PDN}) &= 40\text{mA} \times 2.7\text{V} \\ p(\text{ACT_PDN}) &= 108\text{mW} \end{aligned} \tag{EQ 7}$$

$$\begin{aligned} p(\text{ACT_STBY}) &= 70\text{mA} \times 2.7\text{V} \\ p(\text{ACT_STBY}) &= 189\text{mW} \end{aligned} \tag{EQ 8}$$

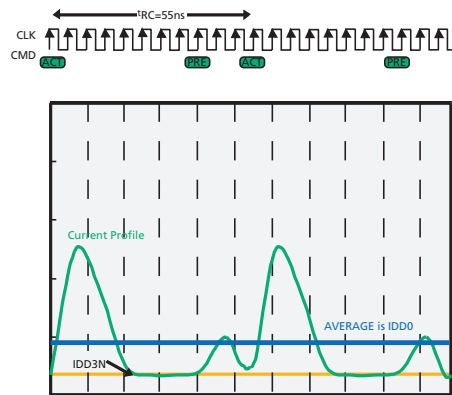
Activate Power

To be useful, a DDR SDRAM must read and write data. In order to complete this task, a row must first be selected using an ACT command, along with a bank and row address. For every ACT command, there is a corresponding PRECHARGE (PRE) command. Where the ACT command opens a row, the PRE command closes the row. While other commands may be present, the ACT and PRE commands are always paired together.

As shown in Figure 3 on page 6, the ACT and PRE commands cause significant activity in the DRAM. The current required for this activity is determined using the I_{DD0} specification in the data sheet. The time between successive ACT commands in the same bank is specified as the minimum t_{RC} .

Figure 3 shows a typical current profile for I_{DD0} . After the ACT command, a large amount of current is used to decode the command/address and then transfer the data from the DRAM array to the sense amplifiers. Once this is complete, the DRAM is maintained in an active state and draws I_{DD3N} until a PRE command is issued. The PRE command restores the data from the sense amplifiers into the memory array and resets the bank for the next ACT command. Once this is complete, the device is returned to the pre-charge state. For I_{DD0} , this cycle is then repeated at t_{RC} intervals between ACT commands.

Figure 3: IDD0 Current Profile



Note: The minimum $t_{RC} = 55\text{ns} = (11 \text{ clock cycles})$.

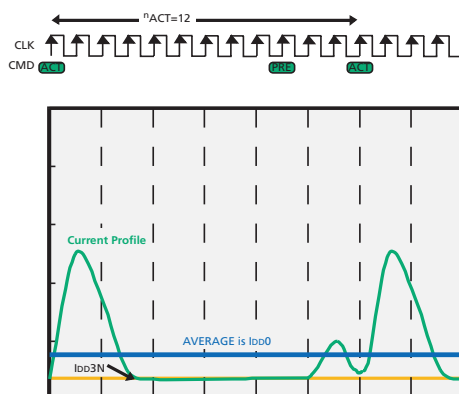
The $IDD0$ value specified in the data sheet is the average current required for device operation. In Figure 3, this is represented by the blue line. During this time, CKE is held HIGH so the device is always drawing a base amount of current ($IDD3N$). This current was calculated as $p(\text{ACT_STBY})$ in Equation 8 on page 5. Therefore, to calculate the power consumed by the ACT-PRE pair, $p(\text{ACT})$, $IDD3N$ must be subtracted from $IDD0$ prior to multiplying by the maximum V_{DD} .

$$\begin{aligned}
 p(\text{ACT}) &= (IDD0 - IDD3N) \times V_{DD} \\
 p(\text{ACT}) &= (135\text{mA} - 70\text{mA}) \times 2.7\text{V} \\
 p(\text{ACT}) &= 175\text{mW} \tag{EQ 9}
 \end{aligned}$$

This equation is correct if the DRAM is only used at minimum t_{RC} cycle time. However, it is unlikely that most systems operate in this manner. Fortunately, it is easy to scale the ACT current for other modes of operation. Two examples of scaling activate power with different activate spacings are shown below: when ACT-ACT cycle time is greater than t_{RC} and when the device is in bank interleave mode.

Refer to Figure 4 for an example where the ACT-ACT cycle time is greater than the minimum specified $t_{RC} = 55\text{ns}$. The t_{RC} is stretched to 12 clock cycles (60ns). A new parameter, n_{ACT} , is used to signify the number of clock cycles between ACT cycles.

Figure 4: ACT-ACT Current with $t_{RC} = 12 t_{CK}$



The I_{DD0} value can easily be scaled as a ratio of the actual ACT-ACT duration to the data sheet conditions. Notice that I_{DD3N} is not scaled. Therefore, it must be subtracted from the ratio. The calculations are as follows:

$$p(\text{ACT}) = (I_{DD0} - I_{DD3N}) \times \frac{t_{RC(\text{spec})}}{n_{\text{ACT}} \times t_{\text{CK}}} \times V_{DD}$$

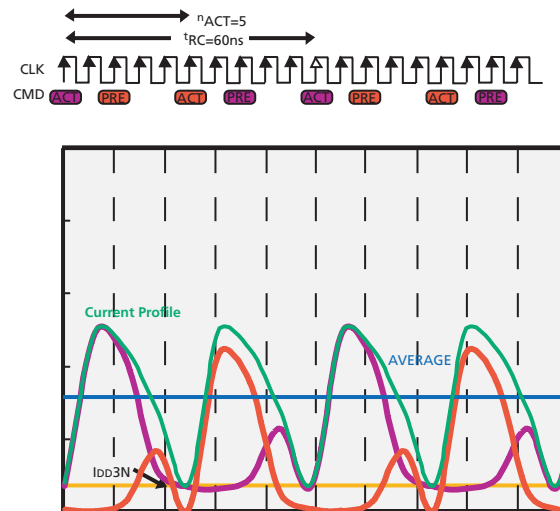
$$p(\text{ACT}) = (135\text{mA} - 70\text{mA}) \times \frac{55\text{ns}}{12\text{CK} \times 5\text{ns/CK}} \times 2.7\text{V}$$

$$p(\text{ACT}) = 161\text{mW} \tag{EQ 10}$$

By changing the ACT-ACT time from $11 t_{\text{CK}}$ to $12 t_{\text{CK}}$, the activation power, $p(\text{ACT})$, drops from 175mW to 161mW . Note that this power is only the activation power and does not include the background power contributed by I_{DD3N} .

Because there are multiple banks on the DDR SDRAM, it is possible to have several banks open at one time. Therefore, it is also possible to have ACT commands closer together than t_{RC} . Figure 5 shows an example where two banks are interleaved. Each bank has $t_{\text{RC}} = 10 t_{\text{CK}}$. Therefore, the average time between ACT cycles is $n_{\text{ACT}} = 5$. The assumption is that the clock is operating at 167MHz , so $t_{\text{CK}} = 6\text{ns}$. The purple current profile is for the first bank activated and includes the I_{DD3N} component. This is only included once on the device even if other banks are open. Therefore, the red current profile, representing the second bank activated, is offset by I_{DD3N} . The green curve represents the summation of the two banks.

Figure 5: ACT-ACT Separation of $4 t_{\text{CK}}$



The calculation to determine the power consumption for only the activation power is the same as before.

$$p(\text{ACT}) = (I_{\text{DD0}} - I_{\text{DD3N}}) \times \frac{t_{\text{RC(spec)}}}{n_{\text{ACT}} \times t_{\text{CK}}} \times V_{\text{DD}}$$

$$p(\text{ACT}) = (135\text{mA} - 70\text{mA}) \times \frac{55\text{ns}}{5\text{CK} \times 6\text{ns}} \times 2.7\text{V}$$

$$p(\text{ACT}) = 322\text{mW} \tag{EQ 11}$$

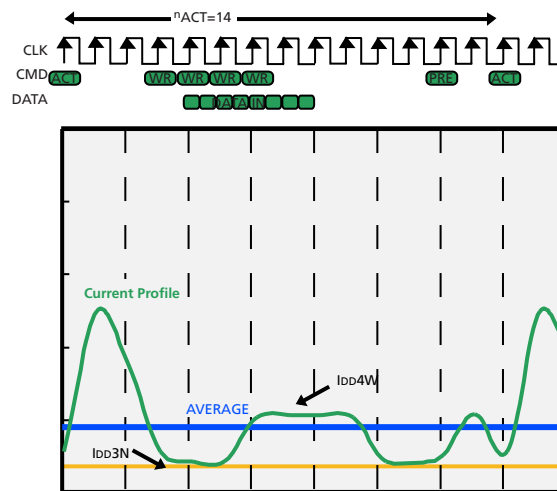
The p(ACT) for two interleaved banks increases from 161mW to 322mW. This is intuitive because twice the amount of ACT and PRE power is consumed when operating two banks compared to one bank.

With this basic equation, the ACT-PRE power can be calculated over any usage condition, from four interleaved banks to one bank that is seldom opened.

Write Power

Once a bank is open, the data can either be read from or written to the DDR SDRAM. The two cases are similar, and the write case will be calculated first. Figure 6 shows an example of a WRITE cycle.

Figure 6: WRITE Cycle



Note: WR = WRITE command with BL = 2 and t_{CK} = 5ns.

As with the ACT-PRE command sequence, the DDR SDRAM uses a peak of power after the ACT command and a smaller amount of current after the PRE command. If a WRITE does not occur, the current consumption remains at I_{DD3N} between these two peaks of current.

However, when several WRITES are added, the consumption of current associated with the WRITE is I_{DD4W}. I_{DD4W} is typically specified as continuous WRITES. The amount of additional power required for the WRITE shown in Figure 6 is calculated as follows:

$$p(\text{WR}) = (\text{IDD4W} - \text{IDD3N}) \times \frac{\text{num of WR cycles}}{n_{\text{ACT}}} \times V_{\text{DD}}$$

$$p(\text{WR}) = (185\text{mA} - 70\text{mA}) \times \frac{4\text{CK}}{14\text{CK}} \times 2.7\text{V}$$

$$p(\text{WR}) = 89\text{mW} \tag{EQ 12}$$

First, the amount of additional current required for the WRITE is calculated by subtracting the background current from the write current ($\text{IDD4W} - \text{IDD3N}$). This current is only used during the WRITE cycles, so it is a ratio of the number of WRITE cycles over the total cycles— t_{ACT} . Finally, this is multiplied by V_{DD} to calculate the device power.

It is now also possible to calculate the total device power, which includes the write power, the ACT power, and the active standby power.

First, the $p(\text{ACT})$ is calculated by substituting Figure 6 values into Equation 10:

$$p(\text{ACT}) = (\text{IDD0} - \text{IDD3N}) \times \frac{t_{\text{RC(spec)}}}{n_{\text{ACT}} \times t_{\text{CK}}} \times V_{\text{DD}}$$

$$p(\text{ACT}) = (135\text{mA} - 70\text{mA}) \times \frac{55\text{ns}}{14\text{CK} \times 5\text{ns/CK}} \times 2.7\text{V}$$

$$p(\text{ACT}) = 138\text{mW} \tag{EQ 13}$$

Recall that $p(\text{ACT_STBY})$ was calculated previously in Equation 8 on page 5, so the three power components can now be added together.

$$p(\text{TOT}) = p(\text{ACT}) + p(\text{WR}) + p(\text{ACT_STBY})$$

$$p(\text{TOT}) = 138\text{mW} + 89\text{mW} + 189\text{mW}$$

$$p(\text{TOT}) = 416\text{mW} \tag{EQ 14}$$

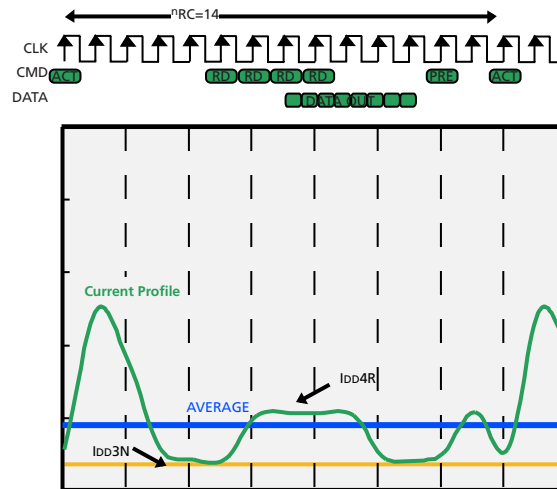
Therefore, to write eight words (four clocks) of data to the DDR SDRAM, with an average cycle time of 14 clocks, requires 416mW of power.

One thing to note is the test conditions for IDD4W . As noted in “Appendix A: Assumptions” on page 18, IDD4W is tested with $\text{BL} = 2$. Often, DDR SDRAMs are operated with burst lengths other than two. If this occurs, the DDR SDRAM generates the additional addresses for the column locations for the subsequent bits in the data burst. The power consumed is still approximated by counting how many clocks of data-in are used for the WRITE. For example, if a WRITE using $\text{BL} = 8$ is completed, it would be the equivalent power of four WRITES with $\text{BL} = 2$ (four clock cycles).

Read Power

The power to read data is similar to that of writing data. The data sheet specifies the read current as I_{DD4R} . A current profile of a READ is shown in Figure 7. In this example, a row is opened with an ACT command and four cycles later, a burst of four READs (two clocks) is started to columns in that row. After the READs are complete, the row is closed with a PRECHARGE command and the sequence is restarted.

Figure 7: Read Current Profile



The read current profile looks very similar to the write current profile. The average current is calculated exactly the same as the write case except I_{DD4R} is substituted for I_{DD4W} .

$$p(\text{RD}) = I_{DD4R} - I_{DD3N} \times \frac{\text{num of RD cycles}}{n_{\text{ACT}}} \times V_{DD}$$

$$p(\text{RD}) = (200\text{mA} - 70\text{mA}) \times \frac{4\text{CK}}{14\text{CK}} \times 2.7\text{V}$$

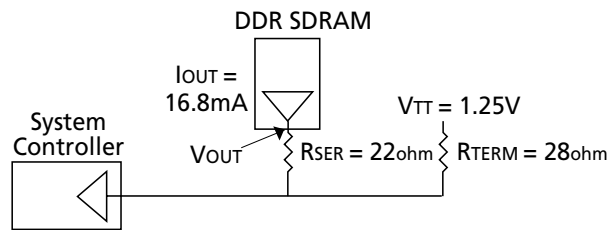
$$p(\text{RD}) = 100\text{mW} \tag{EQ 15}$$

However, this is not the complete answer for the amount of power consumed during a READ. The note attached to I_{DD4R} in Appendix A specifies I_{DD4R} with $I_{OUT} = 0\text{mA}$. Thus, to get the full current consumption for the READ case, the value of I_{OUT} must be calculated.

There are two methods for calculating I_{OUT} . One method is to simulate the data bus in the system using SPICE with models of all components. The power in the output can be determined by averaging a sufficiently long pattern of Pseudo-Random Data. A simpler method is to calculate the DC power of the output driver against the termination. This is usually not worst case, but it provides a first order approximation of the output power.

The DC power calculation will be different for each system, depending on the termination scheme used. A typical DDR SDRAM system is shown in Figure 8. During READs, each output on the DDR SDRAM sinks/sources 16.8mA. The termination consists of a 22 ohm series (typically on the modules) and a 28 ohm series resistor to $V_{TT} = 1.25\text{V}$ (typically on the motherboard).

Figure 8: Typical System DQ Termination



The DC output power is calculated with the output driving a one or zero over multiple clock cycles. This is most easily calculated by determining V_{OUT} first.

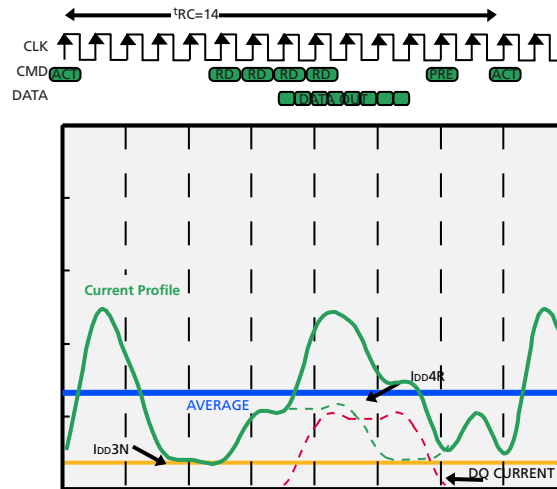
$$\begin{aligned} V_{OUT} &= 1.25V - I_{OUT} \times (R_{SER} + R_{TERM}) \\ V_{OUT} &= 1.25V - 16.8mA \times (22ohm + 28ohm) \\ V_{OUT} &= 0.41V \end{aligned} \tag{EQ 16}$$

The power for the DQs is calculated as shown below. First, the power per output driver, $p(\text{perDQ})$, is calculated as $V_{out} \times I_{out}$. This is multiplied by the number of DQ and DQS pins. This example is assumed to be a x8 device, so there are eight DQs and one DQS. The power includes the power for the DQS signal, which is also driving anytime data is being output. Finally, the total is multiplied by the ratio of RD cycles versus total cycles (same as for write power).

$$\begin{aligned} p(\text{perDQ}) &= V_{OUT} \times I_{OUT} \\ p(\text{perDQ}) &= 0.41V \times 16.8mA \\ p(\text{perDQ}) &= 6.88mW \\ p(\text{DQ}) &= p(\text{perDQ}) \times (\text{num of DQ} + \text{num of DQS}) \times \frac{\text{num of RD cycles}}{n_{ACT}} \\ p(\text{DQ}) &= 6.88mW \times (8 + 1) \times \frac{4CK}{14CK} \\ p(\text{DQ}) &= 17mW \end{aligned} \tag{EQ 17}$$

This output power is consumed while the outputs are actually driving data. Figure 9 shows the current profile if the DQ power is included in a READ cycle. (The dashed green line is the I_{DD4R} line.) To drive the outputs, an additional DQ current is required (and represented by the dashed red line). Adding these two lines together provides the total current profile (solid green line).

Figure 9: Read Current with I/O Power Included



To calculate the total power for this DDR SDRAM READ operation, first determine the activate power using Figure 10 on page 7:

$$p(\text{ACT}) = (\text{IDD0} - \text{IDD3N}) \times \frac{t_{\text{RC}}(\text{spec})}{n_{\text{ACT}} \times t_{\text{CK}}} \times V_{\text{DD}}$$

$$p(\text{ACT}) = (135\text{mA} - 70\text{mA}) \times \frac{55\text{ns}}{14\text{CK} \times 5\text{ns}/\text{CK}} \times 2.7\text{V}$$

$$p(\text{ACT}) = 138\text{mW} \tag{EQ 18}$$

Next, the read power is calculated. Note the I/O power is added to the DDR SDRAM read power, and then the ratio of the number of READ cycles is taken.

Once the subcomponents of the power are determined, they are simply added together, as shown previously. ($p(\text{ACT})$ is from Equation 13 on page 9; $p(\text{RD})$ is from Equation 15 on page 10; $p(\text{DQ})$ is from Equation 17 on page 11; $p(\text{ACT_STBY})$ is from Equation 8 on page 5.)

$$p(\text{TOT}) = p(\text{ACT}) + p(\text{RD}) + p(\text{DQ}) + p(\text{ACT_STBY})$$

$$p(\text{TOT}) = 138\text{mW} + 100\text{mW} + 17\text{mW} + 189\text{mW}$$

$$p(\text{TOT}) = 444\text{mW} \tag{EQ 19}$$

READs, like WRITEs, can be completed with various burst lengths. Although the data sheet is specified with $\text{BL} = 2$, this can be applied to any other burst length. As in the write condition, as long as the actual number of clocks are used for the power ratio, the resulting calculation will approximate the power independent of burst length.

Refresh Power

One final power component must be calculated for an SDRAM to retain data integrity in the system. The memory cells of a DDR SDRAM store the data information in small capacitors that lose their charge over time and must be recharged. This process is called

refresh. The REFRESH operation is normally distributed evenly over time. This is specified assuming the device is in precharge power-down at all times except when the actual REFRESH commands are executed. Thus, the average power for the refresh functionality is:

$$p(\text{REF}) = (\text{IDD5A} - \text{IDD2P}) \times V_{\text{DD}}$$

$$p(\text{REF}) = (6\text{mA} - 4\text{mA}) \times 2.7\text{V}$$

$$p(\text{REF}) = 5\text{mW} \tag{EQ 20}$$

Power Derating

So far, the power calculations have assumed the system was operating at the worst-case VDD. They also assumed the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as p(spec cond). However, most systems operate at different clock frequencies or operating voltages than the ones defined in the data sheet. Each of the power components must be derated to the actual system conditions. The resulting power is noted at P(use cond). (Note: Powers designated with a “p” are worst-case VDD and data sheet clock frequency, while “P” denotes the derated power for system VDD and clock frequency.) The following section explains how to derate each of the power components to the actual system operation.

Voltage Supply Scaling

All power calculations thus far have been calculated at maximum specified VDD. However, few systems operate at such conditions. Systems often operate closer to a nominal VDD. Most of the power components scale as VDD changes. The only power parameter that does not scale with VDD is p(DQ).

On many DRAMs, the power is related to the square of the voltage supply. This is because as voltage is reduced, the operating currents also decrease approximately proportional to the change in VddQ. Therefore, a 5% reduction in VDDQ also reduces the current by approximately 5%, resulting in a 9.8% reduction in power.

Thus, to scale power to a different supply voltage:

$$P(\text{use VDD}) = p(\text{spec VDD}) \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2} \tag{EQ 21}$$

Frequency Scaling

Similarly, many of the power components are dependent on the clock frequency at which the device is operating, including: p(ACT_STBY) (Equation 4 on page 4); p(PRE_STBY) (Equation 2 on page 4); p(WR) (Equation 12 on page 9); and p(RD) (Equation 15 on page 10).

Other powers, such as p(PRE_PDN) and p(ACT_PDN) are not dependent on operating clock frequency because the clock is disabled during power-down mode. p(ACT) is also not clock frequency dependent because it is only dependent on the interval between ACT commands. Similarly, p(REF) does not scale with clock frequency.

For the powers that are operating frequency dependent, the power can be scaled for actual operating frequency:

$$P(\text{use freq}) = p(\text{spec freq}) \times \frac{(\text{use freq})}{(\text{spec freq})} \quad (\text{EQ 22})$$

The use_freq is the actual clock frequency that the device is operating at in the system. The spec_freq is the clock frequency that the device was tested at during the IDD tests. This information is provided in the test condition notes in the data sheet. The notes describe that the device is tested at the minimum clock rate for a specific CAS latency. This value is specified under the ^tCK parameter.

$$P(\text{PRE_PDN}) = p(\text{PRE_PDN}) \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{ACT_PDN}) = p(\text{ACT_PDN}) \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{PRE_STBY}) = p(\text{PRE_STBY}) \times \frac{(\text{use freq})}{(\text{spec freq})} \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{ACT_STBY}) = p(\text{ACT_STBY}) \times \frac{(\text{use freq})}{(\text{spec freq})} \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{ACT}) = p(\text{ACT}) \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{WR}) = p(\text{WR}) \times \frac{(\text{use freq})}{(\text{spec freq})} \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{RD}) = p(\text{RD}) \times \frac{(\text{use freq})}{(\text{spec freq})} \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2}$$

$$P(\text{REF}) = p(\text{REF}) \times \frac{(\text{use VDD})^2}{(\text{max spec VDD})^2} \quad (\text{EQ 23})$$

Calculating Total System Power

The tools are now in place to calculate the system power for any usage condition. The last task is putting them all together. To determine the DDR SDRAM operation of a system, the following components are needed for input.

Table 1: DDR SDRAM Components

Component	Description
Use VDD	System VDD that the device is operating. This is typically closer to a nominal value of 2.5V.
Use freq	Frequency at which the system clock to the DDR SDRAM is operating.
P(perDQ)	The output power of a single DQ (as calculated earlier).
BNK_PRE%	Percentage of time all banks are precharged.
CKE_LO_PRE%	Percent of the banks' PRE time that CKE is LOW.
CKE_LO_ACT%	Percent of the ACT time that CKE is LOW.
^t ACT	The average time between ACT commands.
RD%	Percentage of CK cycles that output read data.
WR%	Percentage of CK cycles that input write data.

There are times when ^tACT is not known for a specific system. In this case, ^tACT can be easily calculated from the RD% and WR% as long as the “Page Hit%” and clock frequency are also known. This calculation is:

$$\begin{aligned}
 \text{COLtoCOL} &= \frac{(\text{BurstLength}/2) \times \text{t}_{\text{CK}}}{(\text{RD}\% + \text{WR}\%)} \\
 \text{t}_{\text{ACT}} &= \frac{\text{COLtoCOL}}{100\% - \text{Page Hit}\%} \quad (\text{EQ 24})
 \end{aligned}$$

The Page Hit% is the number of page accesses that are directed to a row that has already been read from, which has not been precharged. This number may range from 0% for a system operating with a page closed policy up to 60%–80% (or more) for a system operating with efficient page hit rates. As the page hit rate goes up, the average time between ACT commands increases. Also note that as the READ and WRITE bandwidth increases, ^tACT gets shorter. An example of the variation in ^tACT is shown below for a DDR333 device.

Table 2: ^tACT Values for DDR333 Versus Read/Write Bandwidth and Page Hit Rate

Note: Values shown in nanoseconds.

		Page Hit%									
		0%	10%	20%	30%	40%	50%	60%	70%	80%	90%
RD% + WR%	10%	150	167	188	214	250	300	375	500	750	1500
	20%	75	83	94	107	125	150	188	250	375	750
	30%	50	56	63	71	83	100	125	167	250	500
	40%	38	42	47	54	63	75	94	125	188	375
	50%	30	33	38	43	50	60	75	100	150	300
	60%	25	28	31	36	42	50	63	83	125	250
	70%	21	24	27	31	36	43	54	71	107	214
	80%	19	21	23	27	31	38	47	63	94	188
	90%	17	19	21	24	28	33	42	56	83	167
	100%	15	17	19	21	25	30	38	50	75	150

To determine the system power, each of the parameters from Table 1 on page 15 are applied to the equations already discussed. First, the standby/power-down currents are ratioed to actual system use. The equations below are modified from Equation 1, Equation 2, Equation 3, and Equation 4 on page 4, which add the percentages of time the device is precharged and the percentage of time the device is in power-down mode. Note that these numbers cover 100 percent of the total device operating time. During actual device operation (ACTIVATEs, READs, WRITEs), the device is starting from a base power of p(ACT_STBY).

$$\begin{aligned}
 p(\text{PRE_PDN}) &= I_{DD2P} \times V_{DD} \times \text{BNK_PRE\%} \times (\text{CKE_LO_PRE\%}) \\
 p(\text{PRE_STBY}) &= I_{DD2F} \times V_{DD} \times \text{BNK_PRE\%} \times (1 - \text{CKE_LO_PRE\%}) \\
 p(\text{ACT_PDN}) &= I_{DD3P} \times V_{DD} \times (1 - \text{BNK_PRE\%}) \times (\text{CKE_LO_ACT\%}) \\
 p(\text{ACT_STBY}) &= I_{DD3N} \times V_{DD} \times (1 - \text{BNK_PRE\%}) \times (1 - \text{CKE_LO_ACT\%})
 \end{aligned}
 \tag{EQ 25}$$

Next, the activate power is calculated. This is done with a slight variation to Equation 10 on page 7, where ^tACT is substituted for (^tACT x ^tCK). ^tACT is the average cycle time between ACTIVATE commands to the DRAM.

$$p(\text{ACT}) = (I_{DD0} - I_{DD3N}) \times \frac{t_{RC(\text{spec})}}{t_{\text{ACT}}} \times V_{DD}
 \tag{EQ 26}$$

Similarly, Equation 12, Equation 15, and Equation 17 are modified to work with RD% and WR% variables.

$$p(\text{WR}) = I_{\text{DD4W}} - I_{\text{DD3N}} \times \text{WR}\% \times V_{\text{DD}}$$

$$p(\text{RD}) = I_{\text{DD4W}} - I_{\text{DD3N}} \times \text{RD}\% \times V_{\text{DD}}$$

$$p(\text{DQ}) = p(\text{perDQ}) \times (\text{num_of_DQ} + \text{num_of_DQS}) \times \text{RD}\% \quad (\text{EQ 27})$$

The only other power that is calculated is $p(\text{REF})$, as shown in Equation 20 on page 13. No additional modification is required for $p(\text{REF})$.

Now that all the subcomponents of the memory power are calculated, they must be scaled to match the system operating V_{DD} and operating CK frequency. This is done using Equation 20 on page 13, Equation 23 on page 14, and Equation 27 on page 17. Once all the subcomponents are scaled to proper voltage and frequency, they can be added together to provide the total device power consumed.

$$P(\text{TOT}) = P(\text{PRE_PDN}) + P(\text{PRE_STBY}) + P(\text{ACT_PDN}) + P(\text{ACT_STBY}) + P(\text{WR}) + P(\text{RD}) + P(\text{DQ}) + P(\text{REF}) \quad (\text{EQ 28})$$

The total power dissipation of a DDR SDRAM operating under specific system usage conditions has now been calculated, with all primary variables that affect device power having been compensated for.

This can be difficult to do without the proper tools. An Excel spreadsheet is available to facilitate DDR SDRAM memory system power calculations at www.micron.com/system-calc. To utilize this spreadsheet, enter the device data sheet conditions on the “Device Spec” tab. Then enter the system conditions on the “Usage Conditions” tab (refer to Table 1 on page 15). With this information, all of the powers are calculated, the intermittent results shown on the “Power Calcs” tab, and the final results displayed on the “Summary” page (See “Appendix A: Assumptions” on page 18 for examples).

Summary

At first glance at the data sheet, it is difficult to determine how much power a DDR SDRAM will consume in a system environment. However, by understanding the data sheet and how a DDR SDRAM consumes power, it is possible to create a power model based on system usage conditions. A system designer can utilize this model to accurately approximate the power requirements of a DDR SDRAM in a system environment. These results can be used to optimize the system power delivery and thermal budget to optimize performance versus cost of the system.

This model allows a system designer to experiment with various memory access schemes to determine the impact on power consumption. To reduce power, a system designer could consider more aggressive use of power down (CKE is LOW).

A system designer may also use the model to determine increases in power caused by speculatively opening multiple banks or speculatively reading data from an open row. Both techniques can be used to increase system performance at the cost of higher device power. This tool provides a method for estimating the power increase and for making system architecture and design decisions.

By accurately estimating realistic power consumptions, the system designer is able to handle all system trade-offs to optimize the system for its determined use.

Appendix A: Assumptions

Table 3: Data Sheet Assumptions for a 256Mb DDR400 Device

Note 1; $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$

Parameter/Condition	Symbol	-5B	Units
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = 45\text{ns}$; $t_{CK} = 5\text{ns}$; DQ, DM, and DQS inputs changing once every two clock cycles	I _{DD0}	135	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = 5\text{ns}$ MIN; CKE = LOW	I _{DD2P}	4	mA
IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; $t_{CK} = 5\text{ns}$; CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} and V _{REF} for DQ, DQS, and DM	I _{DD2F}	60	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank; Power-down mode; $t_{CK} = 5\text{ns}$; CKE = LOW	I _{DD3P}	40	mA
ACTIVE STANDBY CURRENT: CS# = HIGH; One bank; $t_{CK} = 5\text{ns}$; CKE = HIGH; Address and other control inputs changing once per clock cycle; V _{IN} and V _{REF} for DQ, DQS, and DM	I _{DD3N}	70	mA
OPERATING CURRENT: Burst = 2; READs; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = 5\text{ns}$; I _{OUT} = 0mA	I _{DD4R}	200	mA
OPERATING CURRENT: Burst = 2; WRITEs; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = 5\text{ns}$; DQ, DM, and DQS changing twice per clock cycle	I _{DD4W}	195	mA
AUTO REFRESH CURRENT; $t_{REFC} = 7.8\mu\text{s}^2$	I _{DD5A}	6	mA

- Notes:
1. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with the outputs open.
 2. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{RFC} later.

Appendix B: Examples

Three examples are provided to show how to utilize the Micron System-Power Calculator spreadsheet (see the spreadsheet at: <http://www.micron.com/systemcalc>). The first is for a device in a PC system with a 200 MHz clock under moderate workload. The second is for a PC system with 167 MHz clock under a high-stress workload. The final example is a lower power system operating at 133MHz clock with a low stress workload and aggressive power management.

Example 1: DDR400 Moderate Usage

The first example of calculating DDR SDRAM power in a system environment is for a PC3200 system using x8 devices operating at a clock rate of 200 MHz. The system usage conditions are shown in Table 4.

Table 4: System Usage Conditions

Conditions	Value
V _{DD}	2.6V
CK Frequency	200 MHz
Output Power	6.88mW
Percentage of time all banks are precharged	40%
Percentage of time CKE LOW during precharge	50%
Percentage of time CKE LOW during active	0%
Average time between ACT commands	120ns
Percentage of output cycles reading data	30%
Percentage of output cycles writing data	15%

The system usage assumes that 40 percent of the time all banks on the DDR SDRAM are in a precharge state, and the average time between ACT commands is 120ns. The controller uses a moderate power management scheme during precharge state to keep the device in PDN mode 50 percent of the time. During the active state, power down mode is not utilized. A bus utilization is assumed to be 45 percent with two READs for every WRITE (i.e., the device drives data 30 percent of the time and receives data 15 percent of the time.)

Once these assumptions are input into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition. (This analysis uses the device data sheet from Appendix A.)

Table 5: Power Derated for System Usage Conditions Input Into This Model

Property	Power-Derated Value
p(PRE_PDN)	2.2mW
p(IDLE_STBY)	32.4mW
p(ACT_PDN)	0.0mW
P(ACT_STBY)	113.4mW
p(REF)	5.4mW
p(ACT)	80.4mW
p(WR)	50.6mW
p(RD)	105.3mW
p(DQ)	18.6mW
Total	408.3mW

These results assume data sheet worst-case VDD and data sheet ^tCK specifications. Then the worksheet scales the power to compensate for actual system VDD and clock rate, as shown below:

Table 6: Power Scaled for Actual System CK Frequency and VDD

Property	Scaled Value
P(PRE_PDN)	2.0mW
P(IDLE_STBY)	30.0mW
P(ACT_PDN)	0.0mW
P(ACT_STBY)	105.2mW
P(REF)	5.0mW
P(ACT)	74.6mW
P(WR)	46.9mW
P(RD)	97.6mW
P(DQ)	18.6mW
Total	380.0mW

A summary of the results is shown below. Under these system conditions, 142mW of power is used for the background operations, including all power-down, standby, and refresh powers. An average of 75mW is consumed activating banks, while 163mW is consumed actually reading and writing data to the DDR SDRAM. The summation of these powers shows the total device draws ~380mW of power during a moderate workload.

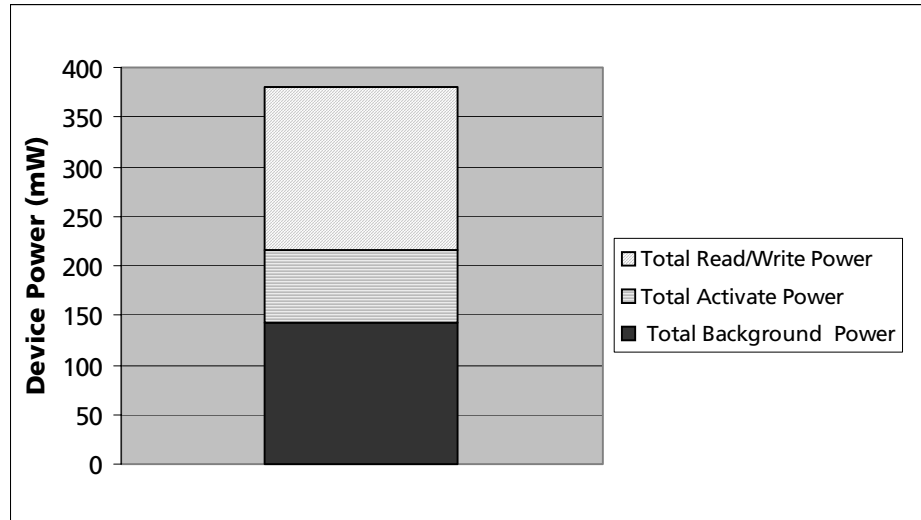
Table 7: Power Consumption Summary

P(PRE_PDN)	2.0mW
P(PRE_STBY)	30.0mW
P(ACT_PDN)	0.0mW
P(ACT_STBY)	105.2mW
P(REF)	5.0mW
Total Background Power	142.2mW
P(ACT)	74.6mW
Total Activate Power	74.6mW
P(WR)	46.9mW
P(RD)	97.6mW
P(DQ)	18.6mW
Total Read/Write Power	163.2mW
Total DDR1 SDRAM Power	380.0mW

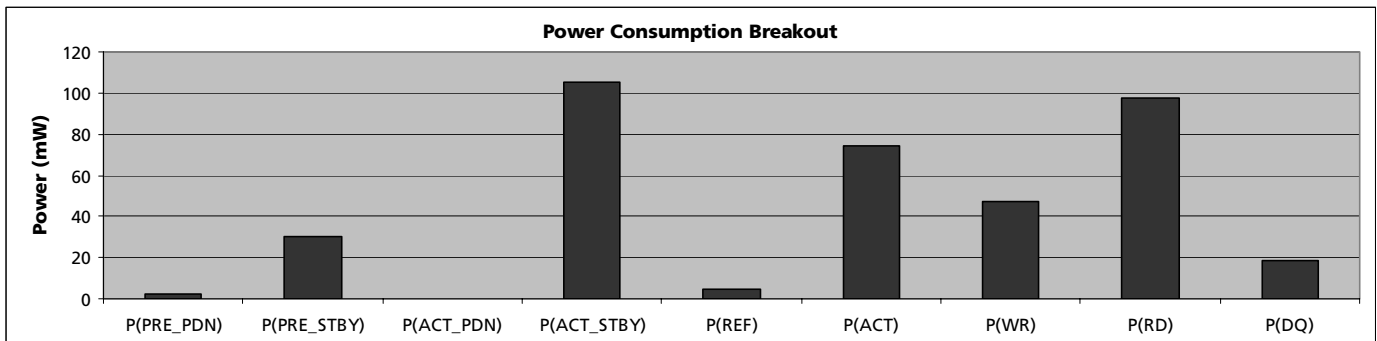
**Output for Example 1: 256Mb DDR SDRAM with 8 DQs and a -5B Speed Grade
(Running at DDR400 speed with a moderate-stress workload)**

System is operating at 200 MHz at VCC = 2.6V. Read bandwidth is 120 Mb/s with write bandwidth of 60 MB/s. The data bus is idle 55 percent of the time. ACT commands are separated by 120ns on average. All parameters are calculated and require no user input.

Power Consumption per Device



Power Consumption Breakout



Example 2: DDR333 High-Stress Workload

The second example is for a PC2700 system that is operating under a high-stress workload. This type of workload would not normally occur in actual system operation. However, with specific benchmarking software or software designed to stress the memory subsystem, conditions like this may be possible. This condition represents a possible worst-case power environment. This type of system is summarized in the following table:

Table 8: System Usage Conditions

Conditions	Value
VDD	2.5V
CK Frequency	167 MHz
Output Power	6.88mW
Percentage of time all banks are precharged	5%
Percentage of time CKE LOW during PRECHARGE	0%
Percentage of time CKE LOW during ACTIVE	0%
Average time between ACT commands	30ns
Percentage of output cycles reading data	80%
Percentage of output cycles writing data	10%

The clock rate is running at 167 MHz. As the memory is being stressed, the device is reading data out 80 percent of the time, while writing only 10 percent of the time. To support this type of data throughput, the banks are being opened and closed quickly and the average duration between ACT commands is only 30ns. The amount of time when all banks are precharged is assumed to be only 5 percent. The final assumption is that to support these throughputs, there is no CKE power management.

For this analysis, the device data sheet is the same as shown in Appendix A and the previous example.

As shown in Table 9 on page 23, the background power is 139mW. This is similar to the previous example because the power saved by the slower clock frequency is offset by the power increase by not utilizing power down mode. The activate power increased to 275mW because banks are opened in quick succession with an average ACT-to-ACT time of 30ns, versus 120ns in the previous example. The read/write power also increased to 274mW due to the higher bus utilization of read data.

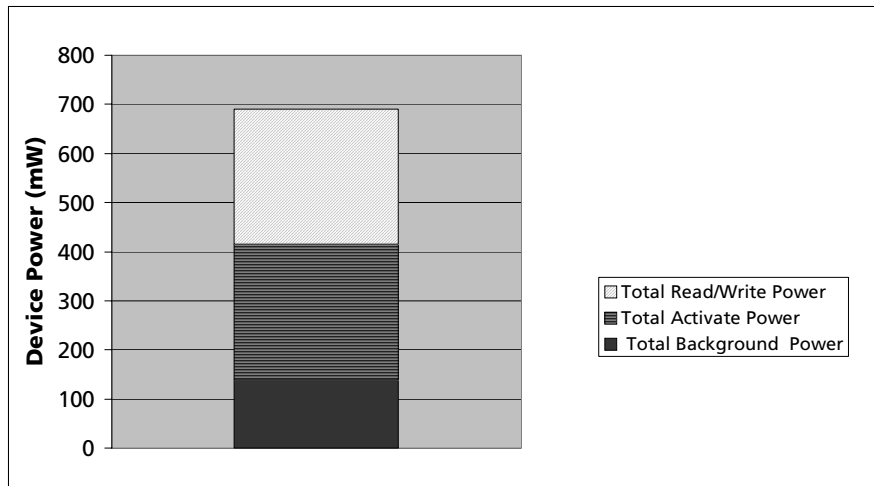
**Output for Example 2: 256Mb DDR SDRAM with 8 DQs and a -5B Speed Grade
(Running at DDR333 with a high-stress workload)**

System is operating at 167 MHz at VCC = 2.5V. Read bandwidth is 268 Mb/s with write bandwidth of 34 MB/s. The data bus is idle 10% of the time. ACT commands are separated by 120ns on average. All parameters are calculated and require no user input.

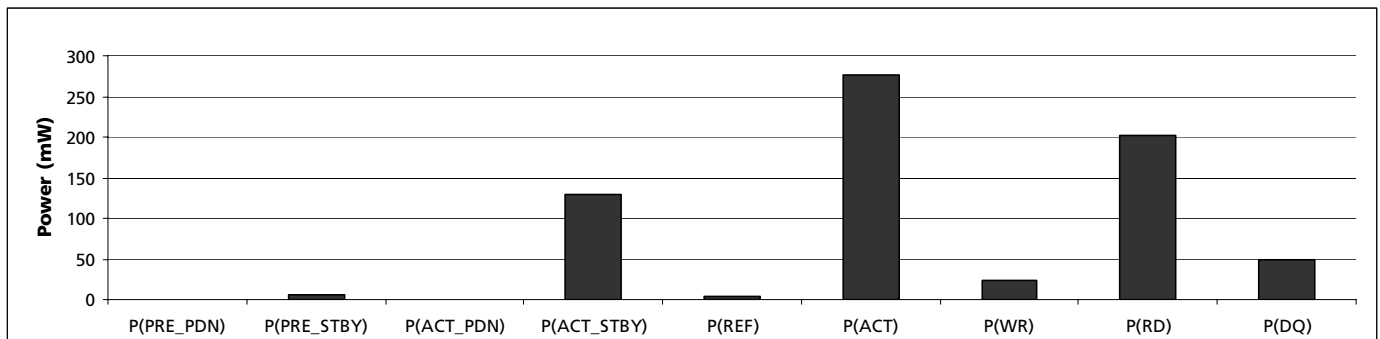
Table 9: Power Consumption Summary

P(PRE_PDN)	0.0mW
P(PRE_STBY)	5.8mW
P(ACT_PDN)	0.0mW
P(ACT_STBY)	128.5mW
P(REF)	4.6mW
Total Background Power	139.0mW
P(ACT)	275.8mW
Total Activate Power	275.8mW
P(WR)	24.2mW
P(RD)	201.0mW
P(DQ)	49.5mW
Total Read/Write Power	274.7mW
Total DDR1 SDRAM Power	689.5mW

Power Consumption per Device



Power Consumption Breakout



Example 3: DDR266 Low-Stress Workload

The third example is for a PC2100 system that is operating under a low-stress workload with aggressive power management. This type of workload would be similar to a mobile design that does not require high bandwidth from the memory. This type of system is summarized in the following table.

The clock rate is running at 133 MHz. As the memory bandwidth requirement is not high, the device is reading data out 10 percent of the time, while writing only 5 percent of the time. This requires ACT commands of only 400ns, and the banks can be precharged 65% of the time. Ample time is also allowed for aggressive use of CKE for further power reduction (CKE is LOW 80 percent of the precharge time and 30 percent of the bank active time).

For this analysis, the device data sheet is the same as shown in Appendix A and the previous example.

Table 10: System Usage Conditions

Conditions	Value
VDD	2.5V
CK Frequency	133 MHz
Output Power	6.88mW
Percentage of time all banks are precharged	65%
Percentage of time CKE LOW during precharge	80%
Percentage of time CKE LOW during active	30%
Average time between ACT commands	400 ns
Percentage of output cycles reading data	10%
Percentage of output cycles writing data	5%

As shown below, almost half of the power consumed is background power. It has been reduced from the previous examples from ~140mW to ~60mW due to lower clock frequency and aggressive use of power down. Due to the lower bandwidth requirements, the activate power and the read/write power also decreased substantially. This allows the total DRAM power consumptions to be approximately 114mW.

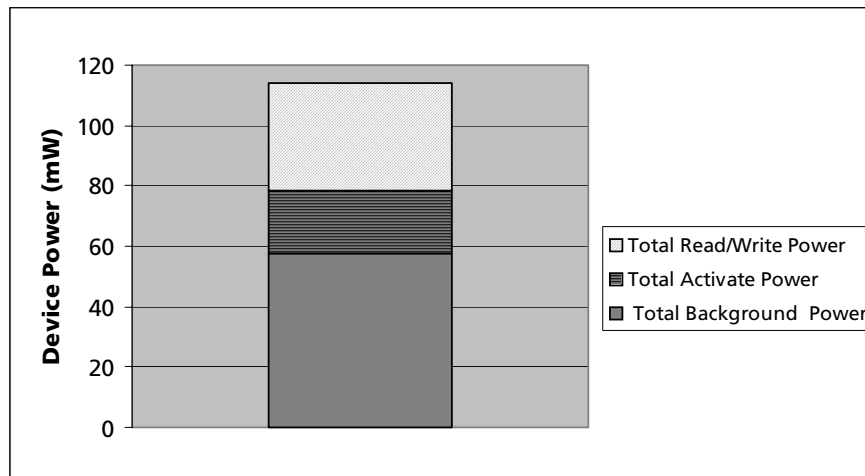
**Output for Example 3: 256Mb DDR SDRAM with 8 DQs and a -5B Speed Grade
(Running at DDR266 with a low-stress workload)**

System is operating at 133 MHz at Vcc = 2.5V. Read bandwidth is 27 Mb/s with write bandwidth of 14 MB/s. The data bus is idle 85% of the time. ACT commands are separated by 400ns on average. All parameters are calculated and require no user input.

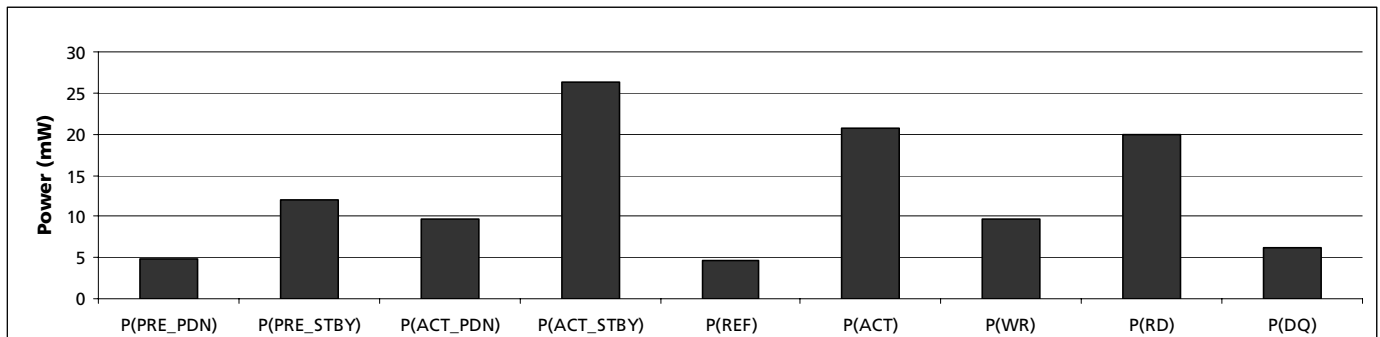
Table 11: Power Consumption Summary

P(PRE_PDN)	4.8mW
P(PRE_STBY)	12.0mW
P(ACT_PDN)	9.7mW
P(ACT_STBY)	26.4mW
P(REF)	4.6mW
Total Background Power	57.6mW
P(ACT)	20.7mW
Total Activate Power	20.7mW
P(WR)	9.6mW
P(RD)	20.0mW
P(DQ)	6.2mW
Total Read/Write Power	35.8mW
Total DDR1 SDRAM Power	114.1mW

Power Consumption per Device



Power Consumption Breakout



Conclusion

These three examples have shown how the power consumption can be calculated for a system. Depending on the how the system accesses the memory, the power consumption rate can vary greatly.

Using the exact same memory, a high-power application can consume as much as 690mW or more, while a lower-power application can consume 115mW or less. For proper system design, it is important that the system architect consider how the DRAM is accessed to ensure the proper considerations when completing the power delivery and thermal solutions.



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